Joyen Benitto

SoC Design Engineer & Computer Architecture Researcher
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Research Interests

- **Computer Architecture:** Architectural, software, and microarchitectural design
- **Domain-Specific Architectures:** Hardware/software codesign optimization
- **Electronic Design Automation (EDA):** SoC automation and verification
- **Microarchitecture:** Performance optimization of architectural components

Experience

SoC Design Engineer Jun'23 – Present
InCore Semiconductors, IIT Madras Research Park

- Develop and Maintain RISC-V SoC generator platform and associated methodologies
- Architected Device Manager, a scalable framework for IP management that automates:
  - Verilog to Bluespec SystemVerilog wrapper generation
  - Test infrastructure and documentation generation
  - Third-party IP integration and maintenance
- Contributed to Azurite, a configurable RISC-V core generator platform
- I work under the supervision of Dr. Neel Gala

Research Contributor Oct'23 – Dec'23
Centre for Heterogeneous and Intelligent Processing Systems, Bangalore

- Contributed to the development of PARISCV, a RISC-V application profiler for custom instruction set optimization
- Research published at OSCAR'24, focusing on hardware-software co-design methodologies
- Conducted research under Dr. Madhura Purnaprajna's supervision

Academic Appointments

Teaching Assistant, RISC-V Architecture Oct'23 – Dec'23
Department of ECE, PES University

- Assisted Prof. Mahesh Awati in teaching RISC-V Architecture
- Conducted tutorial sessions and provided technical guidance

Education

B.Tech in Electronics and Communication Engineering Jun'20 – Jun'24
PES University

- **Research Focus:** Computer Architecture, Hardware-Software Co-design

Publications

[1] **Benitto, J.**, et al. "PARISCV: A Profiler for Application-Specific Acceleration on RISC-V" *OSCAR'24*

[2] **Benitto, J.**, et al. "Enhancing Micro-Strip Patch Antenna Design for HFSS Using a Python Package -'AntGen'." *IEEE MAPCON'23*

Technical Expertise

- **Hardware Description Languages:** SystemVerilog, Bluespec SystemVerilog
- **Programming Languages:** Python, C, CUDA
- **Development Tools:** Git, Linux, Docker, CI/CD

Academic Leadership

Co-Founder, Hyperthrd Computer Architecture Community Oct'23 – Present

- Founded and lead a student-driven research community focused on computer architecture
- Organize technical discussions and research presentations

Technical Mentor, Hackerspace Sep'22 – Dec'23

- Mentored students in hardware development and computer architecture

- Conducted workshops on RISC-V architecture and hardware design

Research Vision

- Drive innovation in EDA and SoC design methodologies
- Develop faster, more efficient, and reliable computing systems
- Bridge the gap between academic research and industry applications
- Contribute to teaching and mentoring in computer architecture

Talks and Lectures

- Understanding Compilers, linkers and loaders with riscv gcc toolchain: Building up from C all the way down to binary using the riscv gcc.
- Coolio with CUDA: A talk introducing CUDA and Data-level parallelism to the audience.
- NVIDIA's Fermi: The First Complete GPU Computing Architecture.
- Datalevel parallelism and a SIMD architectures.
- Understanding RISC-V microarchitecture the simplest way